

AMENDMENTS

IN THE SPECIFICATION

1) page 1, last paragraph, page 2, first paragraph, please replace this text with the following:

a1

In deep submicron CMOS technology, ESD damage has become one of the main reliability concerns. Processing techniques that are applied in advanced CMOS technology procedures can lead to degradation of the performance of ESD circuits that are part of Integrated Circuits (IC's). Examples of these advanced processing techniques are the formation of Lightly Doped Drain (LDD) regions in the MOSFET devices, the formation of salicided drain/source surface regions for MOSFET devices and the formation of extremely thin gate oxide layers underneath the gate electrodes of MOSFET devices. To improve the performance of ESD circuitry of deep submicron CMOS IC's, a number of design methods and approaches have been proposed and applied to I/O cells and Power/Ground cells of semiconductor devices. These methods include ESD protection devices, ESD protection circuits, ESD layout technique and process modifications.

a1
For general industrial applications, the input/output pins of the Integrated Circuits must be able to sustain extreme voltage levels when in contact with an ESD source in excess of 2000 volts. In order to achieve this objective, ESD protection circuits are placed around the I/O pads of the IC's such that these ESD protection circuits protect the IC's against potential ESD damage. The ESD protection circuits shunt the electrostatic charges that originate in the ESD source away from the IC thereby preventing damage to the IC.

2) page 19, last paragraph, page 20, first paragraph, please replace this text with the following:

a2
The phenomenon described above can be simulated by using circuit simulators. For this purpose the ESD protection circuit of the invention, which is shown in Fig. 4, has been designed using a 0.25 μm logic salicide process. The simulator that has been used for this purpose is a simulator known as Hspice. The W/L of M_{ESD} in the circuit of the invention has a channel width of 30 μm and a channel length of 0.5 μm for each finger of M_{ESD} . There are a total of 10 fingers for M_{ESD} resulting in a total channel width of 300 μm . The W/L of M_p of the inverter has a channel width of 25 μm and a channel length of 0.35 μm . The W/L of M_n of the inverter has a channel width of 10 μm and a channel

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length of 0.35 μm . The value of resistance R is 12 Kohm while the value of the capacitance C is 0.5 pF. Simulations under two different operating conditions are required in order to verify the functioning of the circuit of the invention. The first operating conditions represent the ESD overstress conditions where ESD overstress is between the VDD and VSS power rails. The second operating conditions represent the power-on conditions where a voltage of 3.3 Volts exists between the VDD and VSS power rails.

As [3) page 20, last paragraph, page 21, first paragraph, please replace this text with the following:]

The operation of the proposed ESD protection circuit when ESD voltage exists between the VDD and VSS power rails can be explained as follows. The ESD overstress voltage with an amplitude of 8 volts and a rise time of 10 nS is applied between the VDD and VSS power rails. Because the junction breakdown voltage of the PMOS device 32 (Fig. 4) is about 9.5V, M_{ESD} must be turned on before conditions of junction breakdown occur. Otherwise, the ESD pulse detection circuit is of no help in triggering (switching on) M_{ESD} , as a consequence, the ESD level will not be improved. When the voltage at VDD is increased, this voltage is coupled to Ni via capacitor C. After the voltage at